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10/662,725	09/15/2003	Melissa Ann Diercks	138681	1504

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EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,725	DIERCKS ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☒ Claim(s) 3-5, 12, 15-17, 24, & 26 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The term "about" in claims 4 & 16 is a relative term which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The limitation of "2.5 volts peak-to-peak" has been rendered indefinite by the use of the term "about".

2. The term "about" in claims 5, 12, 17, 24 & 26 is a relative term which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The limitation of "10% of magnitude" has been rendered indefinite by the use of the term "about".

3. The term "about" in claim 15 is a relative term which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The limitation of "10 volts peak-to-peak" has been rendered indefinite by the use of the term "about".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 6, 10, & 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Ortiz et al., US 6,631,063.

Ortiz discloses a method of testing an electrical switchgear system, comprising:

- applying an analog signal **8** to a node **81** in said electrical switchgear system (FIG. 8), wherein said node monitors a power line signal and controls a breaker based on said power line signal, and wherein said analog signal simulates said power line signal; and
- receiving data representing a status of said breaker (FIG. 5).

As per Claim 2, Ortiz further discloses the method of testing wherein said data is received from at least one of said node or said breaker (column 5, lines 49-50).

As per Claim 6, Ortiz further discloses the method of testing wherein said applying said analog signal is performed while said node **22** (V_1) monitors said power line signal **17**.

As per Claim 10, Ortiz further discloses the method of testing

- wherein said analog signal is a first analog signal **8** (V_1), said node is a first node **22** (V_1), said breaker is a first breaker **24** (ground line 1), and said power line signal is a first power line signal **17** (line 1),
- wherein said method further comprises applying, simultaneously with said applying said first analog signal **8** (V_1), a second analog signal **8** (V_n) to a second node **22** (V_2) in said electrical switchgear system,
- wherein said second node **22** (V_2) monitors a second power line signal **17** (line 2) and controls a second breaker **24** (ground line 2) based on said second power line signal **17** (line 1), and
- wherein said second analog signal simulates said second power line signal (FIG. 5).

As per Claim 25, Ortiz discloses a storage medium **28** comprising instructions for controlling a processor **20** for testing an electrical switchgear system to:

- apply an analog signal 8 to a node 81 in said electrical switchgear system (FIG. 8), wherein said node monitors a power line signal and

controls a breaker based on said power line signal, and wherein said analog signal simulates said power line signal; an d

- receive data representing a status of said breaker (FIG. 5).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3-5, 7-9;11-24, & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ortiz in view of Baker, US 5,737,168.

As per Claim 3, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose the magnitude of the analog signal of less than about 10 volts peak-to-peak.

Baker discloses the magnitude of the analog signal of less than about 10 volts peak-to-peak (column 11, lines 58-59).

Therefore, it would have been obvious to a person of ordinary skill in the art to limit to test voltage to less than 10 volts, as taught by Baker, in order to avoid damage to the circuit.

As per Claims 4, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose the magnitude of the analog signal of about 2.5 volts peak-to-peak.

Baker discloses the magnitude of the analog signal of about 2.5 volts peak-to-peak (column 11, lines 58-59).

Therefore it would have been obvious to a person of ordinary skill in the art to limit to test voltage to 2.5 volts, as taught by Baker, in order to avoid damage to the circuit.

As per Claim 5, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose the magnitude of the analog signal of less than or equal to about 10% of a magnitude of said power line signal.

Baker discloses the magnitude of the analog signal of less than or equal to about 10% of a magnitude of said power line signal (column 11, lines 58-59).

Therefore it would have been obvious to a person of ordinary skill in the art to limit to test voltage to less than or equal to 10% of the power line voltage, as taught by Baker, in order to avoid damage to the circuit.

As per Claims 7, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose the analog signal to simulate a fault condition of said power line signal.

Baker discloses the analog signal to simulate a fault condition of said power line signal (column 12, lines 1-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply a test signal to simulate a fault condition, as taught by Baker, in order to test the breaker functionality at fault conditions without causing the damage actual high voltage fault could possibly inflict on the circuit.

As per Claims 8, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose the analog signal to simulate a non-fault condition of said power line signal.

Baker discloses the analog signal to simulate a non-fault condition of said power line signal (column 12, lines 1-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply a test signal to simulate a non-fault condition, as taught by Baker, in order to test normal conditions functionality of the breaker.

As per Claims 9, Ortiz discloses a method of testing as applied to Claim 1 above.

Ortiz does not disclose modifying said analog signal based on said status of said breaker; and receiving additional data representing said status of said breaker.

Baker discloses modifying said analog signal based on said status of said breaker; and receiving additional data representing said status of said breaker (column 12, lines 44-47).

Therefore, it would have been obvious to a person of ordinary skill in the art to modify the analog test signal based on the status of the breaker and gather additional information on the status of the breaker, as taught by Baker, in order to tabulate information on the status of the breaker at various times and at various conditions.

As per Claim 11, Ortiz in view of Baker disclose a testing arrangement as applied to Claim 1 above.

Ortiz does not disclose the arrangement further comprising a processor for measuring a time required for the said breaker to trip based on timestamps of said data.

Baker discloses a processor for measuring a time **708** required for the said breaker to trip based on timestamps of said data (column 5, lines 9-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a processor for measuring time, as taught by Baker, in order to evaluate the response time of the breaker.

As per Claim 12, Ortiz discloses a method of testing an electrical switchgear system, comprising:

- applying a first analog signal **8** (V_1) to a first node **22** (V_1) in said electrical switchgear system, wherein said first node monitors a first power line signal **17** (line 1) and controls a first breaker **24** (ground line 1) based on said first power line signal **17** (line 1),
- applying, simultaneously with said applying said first analog signal **8** (V_1), a second analog signal **8** (V_n) to a second node **22** (V_2) in said electrical switchgear system, wherein said second node monitors a second power line signal **17** (line 2) and controls a second breaker **24** (ground line 2) based on said second power line signal **17** (line 2), and
- receiving data from said first node representing a status of said first breaker (FIG. 5).

Ortiz does not disclose:

- and wherein said first analog signal simulates said first power line signal;
- wherein said second analog signal simulates said second power line signal; and
- wherein said first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal.

Baker discloses:

- wherein said first analog signals simulates said first and second power line signals (column 11, lines 54-61);

- wherein said first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal (column 11, lines 58-59).

Therefore, it would have been obvious to a person of ordinary skill in the art to have the analog signals simulate the power line signals, and keep those signals equal to or less then 10% of the power line signal, as taught by Baker, in order to avoid damage to the circuit which could be caused by the high power line voltages.

As per Claim 13, Ortiz discloses an arrangement for testing an electrical switchgear system, comprising:

- an application an analog signal to a node in said electrical switchgear system, wherein said node monitors a power line signal and controls a breaker based on said power line signal, and wherein said analog signal simulates said power line signal; and
- an interface for receiving data representing a status of said breaker.

Ortiz does not disclose a generator for applying the analog signal.

Baker discloses a generator for applying the analog signal (column 2, lines 56-57).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a generator for applying the analog signal, as taught by Baker, in order to regulate the signal.

As per Claim 14, Ortiz in view of Baker discloses the testing arrangement as applied to Claim 13 above. Ortiz further discloses an interface which receives said data from at least one of said node or said breaker (column 5, lines 49-50).

As per Claim 15, Ortiz in view of Baker disclose an arrangement for testing as applied to Claim 13 above.

Ortiz does not disclose the magnitude of the analog signal of less than about 10 volts peak-to-peak.

Baker discloses the magnitude of the analog signal of less than about 10 volts peak-to-peak (column 11, lines 58-59).

Therefore it would have been obvious to a person of ordinary skill in the art to limit to test voltage to less than 10 volts, as taught by Baker, in order to avoid damage to the circuit.

As per Claim 16, Ortiz in view of Baker disclose an arrangement for testing as applied to Claim 13 above.

Ortiz does not disclose the magnitude of the analog signal of about 2.5 volts peak-to-peak.

Baker discloses the magnitude of the analog signal of about 2.5 volts peak-to-peak (column 11, lines 58-59).

Therefore it would have been obvious to a person of ordinary skill in the art to limit to test voltage to 2.5 volts, as taught by Baker, in order to avoid damage to the circuit.

As per Claim 17, Ortiz in view of Baker disclose an arrangement for testing as applied to Claim 13 above.

Ortiz does not disclose the magnitude of the analog signal of less than or equal to about 10% of a magnitude of said power line signal.

Baker discloses the magnitude of the analog signal of less than or equal to about 10% of a magnitude of said power line signal (column 11, lines 58-59).

Therefore, it would have been obvious to a person of ordinary skill in the art to limit to test voltage to less than or equal to 10% of the power line voltage, as taught by Baker, in order to avoid damage to the circuit.

As per Claim 18, Ortiz in view of Baker disclose an arrangement for testing as applied to Claim 13 above. Ortiz further discloses, the application of said analog signal while said node **22** (V_1) monitors said power line signal **17**. The use of the generator to apply the signal is discloses by Baker (Claim 13) above.

As per Claims 19, Ortiz in view of Baker disclose a testing arrangement as applied to Claim 13 above.

Ortiz does not disclose the analog signal to simulate a fault condition of said power line signal.

Baker discloses the analog signal to simulate a fault condition of said power line signal (column 12, lines 1-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply a test signal to simulate a fault condition, as taught by Baker, in order to test the breaker functionality at fault conditions without causing the damage actual high voltage fault could possibly inflict on the circuit.

As per Claims 20, Ortiz in view of Baker disclose a testing arrangement as applied to Claim 13 above.

Ortiz does not disclose the analog signal to simulate a non-fault condition of said power line signal.

Baker discloses the analog signal to simulate a non-fault condition of said power line signal (column 12, lines 1-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply a test signal to simulate a non-fault condition, as taught by Baker, in order to test normal conditions functionality of the breaker.

As per Claim 21, Ortiz in view of Baker disclose a testing arrangement as applied to Claim 13 above.

Ortiz does not disclose modifying said analog signal based on said status of said breaker; and receiving additional data representing said status of said breaker.

Baker discloses modifying said analog signal based on said status of said breaker; and receiving additional data representing said status of said breaker (column 12, lines 44-47).

Therefore, it would have been obvious to a person of ordinary skill in the art to modify the analog test signal based on the status of the breaker and gather additional information on the status of the breaker, as taught by Baker, in order to tabulate information on the status of the breaker at various times and at various conditions.

As per Claim 22, Ortiz further discloses an arrangement:

- wherein said analog signal is a first analog signal **8** (V_1), said node is a first node **22** (V_1), said breaker is a first breaker **24** (ground line 1), and said power line signal is a first power line signal **17** (line 1),
- wherein said generator is also for applying, simultaneously with said applying said first analog signal **8** (V_1), a second analog signal **8** (V_n), to a second node **22** (V_2) in said electrical switchgear system,
- wherein said second node **22** (V_2) monitors a second power line signal and controls a second breaker based on said second power line signal **17** (line 2), and
- wherein said second analog signal simulates said second power line signal (FIG. 5).

As per Claim 23, Ortiz in view of Baker disclose a testing arrangement as applied to Claim 13 above.

Ortiz does not disclose the arrangement further comprising a processor for measuring a time required for the said breaker to trip based on timestamps of said data.

Baker discloses a processor for measuring a time **708** required for the said breaker to trip based on timestamps of said data (column 5, lines 9-12).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a processor for measuring time, as taught by Baker, in order to evaluate the response time of the breaker.

As per Claim 24, Ortiz discloses an arrangement for testing an electrical switchgear system, comprising:

- an application of a first analog signal **8** (V_1) to a first node **22** (V_1) in said electrical switchgear system, wherein said first node monitors a first power line signal **17** (line 1) and controls a first breaker **24** (ground line 1) based on said first power line signal **17** (line 1);
- an application, simultaneously with said applying said first analog signal **8** (V_1), a second analog signal **8** (V_n) to a second node **22** (V_2) in said electrical switchgear system, wherein said second node monitors a second power line signal **17** (line 2) and controls a second breaker **24** (ground line 2) based on said second power line signal **17** (line 2);
- an interface for receiving data from said first node representing a status of said first breaker (FIG. 5).

Ortiz does not disclose:

- the use of a generator;
- the first and second analog signals simulates said first and second power line signals;
- the first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal.

Baker discloses:

- the use of a generator (column 2, lines 56-57)
- the first and second analog signals simulates said first and second power line signals (column 11, lines 54-61);
- the first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal (column 11, lines 58-59.

Therefore, it would have been obvious to a person of ordinary skill in the art to have the analog signals simulate the power line signals, and keep those signals equal to or less then 10% of the power line signal, as taught by Baker, in order to avoid damage to the circuit which could be caused by the high power line voltages. The use of the generator to apply the signal is discloses by Baker as in Claim 13 above.

As per Claim 26, Ortiz discloses a storage medium **28** comprising instructions for controlling a processor **20** for testing an electrical switchgear system to:

- apply a first analog signal **8** (V_1) to a first node **22** (V_1) in said electrical switchgear system, wherein said first node monitors a first power line signal **17** (line 1) and controls a first breaker based **24** (ground line 1) on said first power line signal **17** (line 1);
- apply, simultaneously with said applying said first analog signal **8** (V_1), a second analog signal **8** (V_n) to a second node **22** (V_2) in said electrical switchgear system, wherein said second node monitors a second power line signal **17** (line 2) and controls a second breaker **24** (ground line 2) based on said second power line signal **17** (line 2);
- receive data from said first node representing a status of said first breaker (FIG. 5),

Ortiz does not disclose:

- wherein the first and second analog signals simulate the first and second power line signals;
- wherein said first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal.

Baker discloses:

- wherein the first and second analog signals simulate the first and second power line signals (column 11, lines 54-61);
- wherein said first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal (column 11, lines 58-59).

Therefore, it would have been obvious to a person of ordinary skill in the art to have the analog signals simulate the power line signals, and keep those signals equal to or less then 10% of the power line signal, as taught by Baker, in order to avoid damage to the circuit which could be caused by the high power line voltages.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fasullo et al., US 6,169,649, discloses a method of monitoring a protection device such as a circuit breaker, where a signal is applied to the system and then further monitored by a sensing and detection circuit, the output of which is sent to a controller such as a PC. Burton et al., US 4,814,712, discloses a testing arrangement for a circuit breaker controlled by a microcomputer with a human operator control, which tests power lines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571)272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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